IN THE CLAIMS

1. (Currently amended) A method for forming wire lines and interconnecting contacts, the method comprising;

depositing a wire line layer;

depositing a multi-layered hard mask layer on the wire line layer, the multi-layered hard mask layer including at least a first hard mask layer, a second hard mask layer, and a third hard mask layer, each of ~~which are~~ the first, second, and third hard mask layers formed of different insulating materials to have an etch selectivity with respect to each other;

patterning the multi-layered hard mask layer using a photoresist pattern to produce a multi-layered hard mask;

patterning the wire line layer using the multi-layered hard mask to form wire lines;

filling gaps between the wire lines with an insulating layer; and

forming interconnecting contacts that align with the wire lines and vertically penetrate the insulating layer where the first hard mask is protected by the second hard mask.

2. (Original) The method of claim 1, wherein the wire line layer is a bit line layer, and the interconnecting contacts are capacitor contacts configured to electrically connect the device and capacitors to be formed over the bit lines.

3. (Original) The method of claim 1, wherein the second hard mask comprises an insulating material having an etch selectivity with respect to the insulating layer.

4. (Currently amended) A method for forming wire lines and interconnecting contacts, the method comprising:

forming a wire line layer;

forming a multi-layered hard mask on the wire line layer, the multi-layered hard mask including at least a first hard mask, a second hard mask, and a third hard mask, which are formed of different insulating materials to have an etch selectivity with respect to each other;

forming wire lines by patterning the wire line layer using the multi-layered hard mask;

forming an insulating layer to fill gaps between the wire lines;

forming openings to be aligned with the wire lines and vertically penetrate the insulating layer where the first hard mask disposed on the wire lines is protected by the second hard mask;

forming insulating spacers on the sidewalls of the openings;

forming a conductive layer to fill the openings; and

forming interconnecting contacts that electrically connect the wire line layer to an active region of a semiconductor substrate by filling the openings and by node-separating the conductive layer.

5. (Original) The method of claim 4, wherein the second hard mask layer is formed of at least an insulating material having an etch selectivity with respect to the insulating layer.

6. (Original) A method for forming wire lines and interconnecting contacts, the method comprising:

forming a bit line layer on a first insulating layer;

forming a multi-layered hard mask on the bit line layer, the multi-layered hard mask including at least a first hard mask, a second hard mask, and a third hard mask, each of which are formed of different insulating materials to have an etch selectivity with respect to each other;

patterning the bit line layer using the third hard mask as an etch mask to form bit lines;

forming a second insulating layer on the third hard mask to fill gaps between the bit lines;

forming openings to be aligned with the bit lines and vertically penetrate the second insulating layer and the first insulating layer where the first hard mask disposed on the bit lines is protected by the second hard mask;

forming insulating spacers on the sidewalls of the openings;

forming a conductive layer to fill the openings; and

forming interconnecting contacts filling the openings by node-separating the conductive layer.

7. (Original) The method of claim 6, wherein the bit line is formed of tungsten.

8. (Original) The method of claim 6, further comprising forming a barrier layer including a titanium/titanium nitride layer under the bit line layer.

9. (Original) The method of claim 6, wherein forming the multi-layered hard mask comprises:

sequentially forming a first hard mask layer, a second hard mask layer, and a third hard mask layer on the bit line layer;

forming the third hard mask by patterning the third hard mask layer; and

patterning the second hard mask layer and the first hard mask layer by using the third hard mask as an etch mask.

10. (Original) The method of claim 6, wherein the first hard mask layer is formed to a thinner thickness than the third hard mask layer.

11. (Original) The method of claim 10, wherein the first hard mask layer is formed of silicon nitride.

12. (Original) The method of claim 10, wherein the third hard mask layer is formed of silicon oxide.

13. (Original) The method of claim 6, wherein the second hard mask layer comprises an insulating material having an etch selectivity with respect to the second insulating layer.

14. (Original) The method of claim 13, wherein the second hard mask layer is formed of one of polysilicon and titanium nitride.

15. (Original) The method of claim 6, wherein forming openings comprises:

forming a bar-type photoresist pattern on the second insulating layer to intersect the bit lines or forming a photoresist pattern on the second insulating layer to have circular exposed portions such that the openings are formed to be circular; and

selectively etching exposed portions of the second insulating layer by using the photoresist pattern as an etch mask.

16. (Original) The method of claim 6, wherein the insulating spacer is formed of silicon oxide.

17. (Original) The method of claim 6, wherein the conductive layer is formed of conductive polysilicon.

18. (Original) The method of claim 6, wherein forming interconnecting contacts comprises:

removing the second hard mask by using the first hard mask as an etch stopper; and

node-separating the conductive layer using etching.

19. (Original) The method of claim 18, wherein node-separating the conductive layer using etching comprises one chosen from the group consisting of spin processing and chemical mechanical polishing.

20. (Original) The method of claim 6, wherein the interconnecting contacts are capacitor contacts configured to be electrically connected to capacitors formed over the bit lines.

21-25. (Cancelled)